Abstract

A network processor or other type of processor includes a packet analyzer and first memory circuitry operatively coupled to the packet analyzer. The packet analyzer is operative to at least partially analyze one or more packets received by the processor in order to determine for a given one of the packets a portion of the packet to be stored in the first memory circuitry. The portion of the given packet when stored in the first memory circuitry is thereby made accessible for subsequent processing within the processor, without requiring access to second memory circuitry associated with the processor and configured to store substantially the entire given packet. The packet analyzer may be configured to utilize a value stored in a register of the processor to determine the portion of the given packet to be stored in the first memory circuitry. The register may be one of a number of registers which implement a look-up table accessible to the packet analyzer. The look-up table includes multiple entries, each having packet categorizing information, such as port number or packet flow identifier, and an associated number of blocks of the packet to be stored in the first memory circuitry. The value stored in a given one of the registers may be dynamically updatable under control of a host device operatively coupled to the processor.